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Ohmic contact formation process on low n-type gallium arsenide (GaAs) using indium gallium zinc oxide (IGZO)

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ABSTRACT

Here, an excellent non-gold Ohmic contact on low n-type GaAs is demonstrated by using indium gallium zinc oxide and investigating through time of flight-secondary ion mass spectrometry, X-ray photoelectron spectroscopy, transmission electron microscopy, *J*–*V* measurement, and *H* [enthalpy], *S* [entropy], *Cp* [heat capacity] chemistry simulation. In is diffused through GaAs during annealing and reacts with As, forming InAs and InGaAs phases with lower energy bandgap. As a result, it decreases the electron barrier height, eventually increasing the reverse current. In addition, traps generated by diffused O atoms induce a trap-assisted tunneling phenomenon, increasing generation current and subsequently the reverse current. Therefore, an excellent Ohmic contact with 0.15 A/cm^2 on-current density and 1.5 on/off-current ratio is achieved on n-type GaAs.

1. Introduction

III–V compound semiconductor materials such as GaAs, InGaAs, and GaSb are recently considered as potential candidates for next generation metal oxide semiconductor field effect transistors (MOSFETs) beyond the era of silicon (Si) technology, due to their low effective mass and high carrier mobility [1]. One of the challenging tasks for realizing high-performance III–V MOSFETs is to reduce the high contact resistance for it occupies most of the total parasitic resistance in sub-50 nm technology nodes. Thus, nanometer-scale III–V MOSFETs strongly depend on the quality of junction and body contacts to accomplish high performance. For the past decades, Au/Ge and Pd/Ge have been used as the major Ohmic contact systems applicable for n-type As-based III–V compound semiconductors [2]. Tahamtan et al. reported Au/Ge/Ni Ohmic contact on gallium arsenide (GaAs) with doping concentration of about 10^{18} cm^{-3} by forming interfacial compounds such as NiAs and AuGa [3]. Chang et al. also demonstrated non-gold Ohmic contact using Pd/Ge/Ti/Pt layers on 2×10^{18} cm^{-3} n-type indium gallium arsenide (InGaAs) [4]. In both of the studies, however, the contacts were formed on highly doped GaAs and InGaAs substrates where the depletion width is narrow and consequently high electron tunneling phenomenon occurs from metal to semiconductor. Therefore, a challenge still remains in making an Ohmic contact on low n-type doped GaAs substrates to resolve high contact resistance problem due to poor source/drain (S/D) dopant activation [5]. In this letter, we propose a method to fabricate non-gold Ohmic contact on a low n-type GaAs substrate ($\sim 4 \times 10^{16}$ cm^{-3}) with indium gallium zinc oxide (IGZO). The results are systematically investigated through time of flight secondary ion mass spectroscopy (TOF-SIMS), chemical simulation, X-ray photoelectron spectroscopy (XPS), transmission electron microscopy (TEM), and current density–voltage (*J*–*V*) analyses.

2. Experimental

(1 0 0) n-Type GaAs substrates with doping concentration of 4×10^{16} cm^{-3} were initially cleaned with acetone and methanol for 1 min. Then, the native oxide layer was removed by 10% hydrochloric acid (HCl) dip for 10 min, followed by isopropyl alcohol (IPA) rinse for 10 s. After the cleaning process, about 10 nm thick IGZO layer was deposited on the GaAs substrates in a RF sputtering system (Ar:O_2 = 15:7, 150 W, and 2.5 mTorr). The samples were annealed at 400 °C, 500 °C, and 600 °C for 1 h in a N_2 ambient, followed by 50 nm thick titanium (Ti) and 100 nm thick aluminum (Al) contact metal layers deposition by thermal evaporator through a shadow mask. TOF-SIMS, XPS, TEM, and *J*–*V* analyses were performed on the junction samples to investigate respectively the distribution of elements in the IGZO/GaAs junction interface and their electrical characteristics. In addition,

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in order to predict thermal reactions at the interface between IGZO and GaAs, Gibb's oxidation free energy was simulated by HSC (*H* [enthalpy], *S* [entropy], and *Cp* [heat capacity]) chemistry software.

3. Results and discussion

In order to precisely investigate the distribution of elements in the IGZO/n-GaAs junction interface, TOF-SIMS analysis was conducted. Fig. 1 shows the intensity profiles of ^{16}O, ^{64}Zn, ^{69}Ga, ^{75}As, and ^{115}In atoms in as-deposited and 600 °C annealed samples. Here, the IGZO/n-GaAs interface is defined as the location where Zn and O profiles begin decreasing. In the as-deposited sample, In and As atoms seem to have slightly diffused due to substrate temperature increased during sputter process. After annealing the IGZO/n-GaAs sample at 600 °C, In, Zn, and O atoms were deeply diffused toward n-GaAs bulk region, increasing their overall concentration.

For further understanding on the SIMS data, Gibb's oxidation free energies were calculated by HSC chemistry simulator. As shown in Fig. 2(a), the oxidation free energy of In, Ga, and Zn per 1 mol O in IGZO was calculated under the following reactions, $4In + 3O_2 = 2In_2O_3$, $4Ga + 3O_2 = 2Ga_2O_3$, and $2Zn + O_2 = 2ZnO$. At the chosen range of process temperature (0–600 °C), In_2O_3 always has higher oxidation free energy than Ga_2O_3 and ZnO, consequently indicating that it is in an unstable state and can be easily deoxidized in IGZO. As already observed in the previous SIMS data, the In and O atoms diffused toward the n-GaAs bulk region are expected to be deoxidized during the 600 °C anneal. Especially, O atoms seem to diffuse more deeply because of their high diffusivity in GaAs, compared to that of In [6]. Fig. 2(b) shows a simulated stable phase equilibrium composition (mol %) as a function of temperature when Ga, As, In, Zn, and O atoms are mixed with identical quantity. InAs has a higher simulated stable phase equilibrium composition value than GaAs between 0 °C and 600 °C, meaning that the diffused In atoms are most likely to react with As atoms in the GaAs region. Although InGaAs phase was not taken into account during HSC chemistry simulation for it was not provided by the simulator, it could be inferred that InGaAs has also a higher stable phase equilibrium composition. Since InGaAs has lower band gap with increasing the fraction of In to Ga [7], the InAs and GaInAs phases, which are expected to be newly formed at the surface of GaAs substrate after the anneal process, can reduce the electron barrier height and also increase the reverse current of Schottky junction diode. In addition, as shown in Fig. 2(b), Ga_2O_3 seems to have about 30 mol % equilibrium composition value even though As_2O_3 is non-existent. It is thought that the diffused O atoms most likely reacted with Ga, providing Ga_2O_3 and leaving As atoms near the interface region.

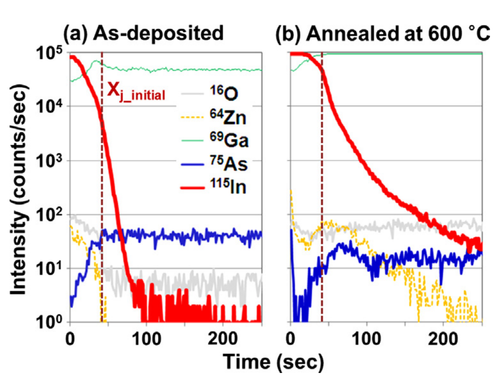

Fig. 1. (a) TOF-SIMS intensity profiles of ^{16}O, ^{64}Zn, ^{69}Ga, ^{75}As, and ^{115}In atoms as a function of profiling time in the IGZO/n-GaAs samples (a) non-annealed and (b) annealed at 600 °C for 1 h.

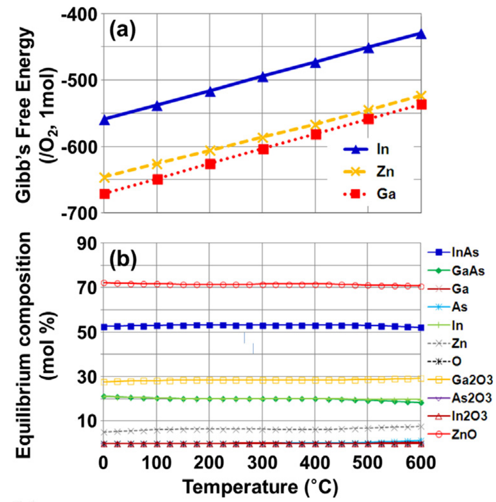

Fig. 2. HSC chemistry simulation. (a) [Oxidation Gibb's free energy] Enthalpy changes of oxidation reactions as a function of annealing temperature. It is assumed that each element exists independently and no interactions. (b) [Phase equilibrium] Stable phase equilibrium composition (mol %) as a function of annealing temperature. It is assumed that the same amount of all elements (Ga, As, In, Zn, and O) are mixed in the system.

In order to validate the formation of InAs or InGaAs as shown in Fig. 3, XPS analysis was additionally performed on GaAs, non-annealed IGZO/GaAs, and 600 °C annealed IGZO/GaAs samples. For the As 3d peak in the GaAs sample, As–O bond (in the form of As_2O_3) and As–Ga bond were respectively observed at 44 eV and 40.7 eV, which are due to As–Ga bond destruction at the surface by native oxidation process in ambient air [8]. The As–O and As–Ga bonds were still present after depositing IGZO film on the GaAs

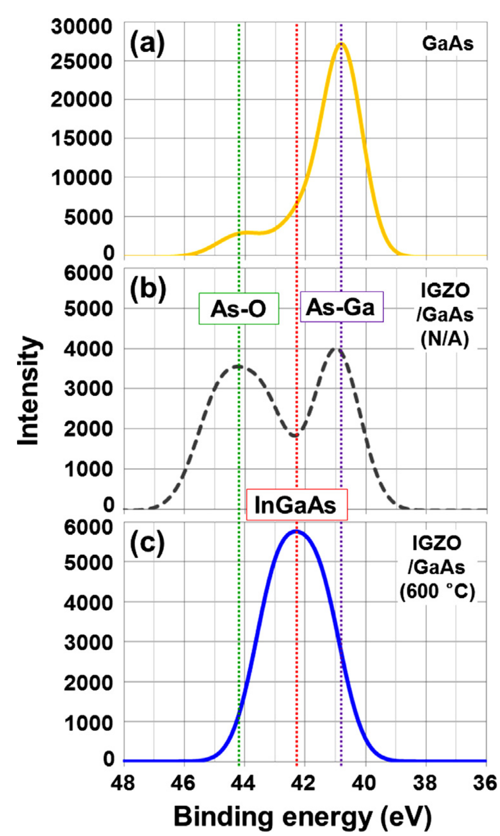

Fig. 3. XPS analysis. The As 3d photoelectron spectra of (a) bare GaAs, (b) IGZO/GaAs before annealing, and (c) IGZO/GaAs after annealing at 600 °C.

substrate, even though the peak intensity of As–Ga was reduced by about one-fifth due to the IGZO blocking layer. Especially, As–O peak intensity was not much reduced because of oxidation on GaAs surface by O_2 ambient during IGZO sputtering process, consequently resulting in As_2O_3 at ~45 eV and As_2O_5 at ~46 eV. As a result, the XPS peak related to As–O was broadened up to 46 eV region in the IGZO/GaAs sample, compared to the control GaAs. However, a different As 3d peak with binding energy of 42 eV was observed in the 600 °C annealed sample, indicating that a new InGaAs phase has formed [9]. According to this XPS data, as already discussed, the 600 °C annealing process seems to enhance the deoxidation of In_2O_3 and subsequently the reaction between In and GaAs. This newly formed InGaAs region was also confirmed by TEM analysis in Fig. 4. About 80–100 nm thick poly-crystalline InGaAs layer was observed near the surface region and 8 nm thick IGZO layer was still remained after the thermal reaction.

Finally, as shown in Fig. 5(a), *J–V* characteristics of annealed Ti/IGZO/n-GaAs junction samples were measured and compared with those of non-annealed Ti/IGZO/n-GaAs and Ti/n-GaAs junction samples. On/off-current ratio and on-current density of the Ti/IGZO/n-GaAs and Ti/n-GaAs junction diodes were extracted and plotted in Fig. 5(b). The non-annealed Ti/n-GaAs Schottky junction has very high on/off-current ratio (~7.2×10^4) because of high electron barrier height achieved by Fermi level pinning phenomenon [10]. Here, the on/off-current ratio was obtained by using a forward current at 2 V and a reverse current value at −2 V. The non-annealed Ti/IGZO/n-GaAs junction is shown to have a lower on-current density (75 times lower) due to the insertion of IGZO film with high resistivity. The contribution of Ti/n-IGZO junction in the Ti/IGZO/n-GaAs samples to the *J–V* characteristics can be ignored because the junction with fairly low electron barrier height normally works as Ohmic contact [11]. In addition, large amount of traps seem to have induced generation current (I_G) in the IGZO/n-GaAs interface resulting in a lower on/off-current ratio (~1.2×10^3), compared to the control sample. The resistivity of IGZO film is known to be reduced after anneal above 400 °C because of its increased carrier mobility [12]. As a result, after performing the annealing process above 400 °C, the higher on-current density was observed and eventually much higher value (0.15 A/cm^2) was obtained in the 600 °C annealed sample than the control. We note that the low on-current densities observed in all IGZO/GaAs junctions including the control are attributed to the high series resistance in the GaAs body substrate. The on/off-current ratio was also reduced after the annealing process because of two reasons: (1) low electron barrier height achieved by decreasing the energy bandgap of the interface material (GaAs) and (2) the newly introduced traps that induces I_G. The In atoms that have diffused into GaAs region seem to form InAs and InGaAs with a lower energy bandgap at the interface that reduces the electron barrier height. In addition, the diffused O atoms from IGZO to GaAs and the remaining As atoms after the reaction between the diffused O and Ga are expected to act as traps in the junction interface that increases the off-current. O atoms are highly reactive to other elements and results in the formation of complex defect (Ga–O–Ga) at the junction. This consequently works as deep carrier traps (0.55 eV below the conduction band) in GaAs. As a result, an excellent Ohmic contact with high on-current density and low on/off-current ratio was achieved in the 600 °C annealed sample by inserting IGZO layer between Ti and GaAs and also annealing to form alloys with low energy bandgap and generate traps that induces generation current in the junction interface.

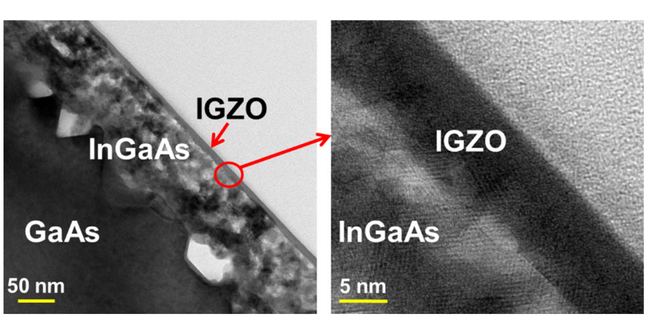

Fig. 4. Cross-sectional TEM images of the 600 °C annealed IGZO/GaAs sample.

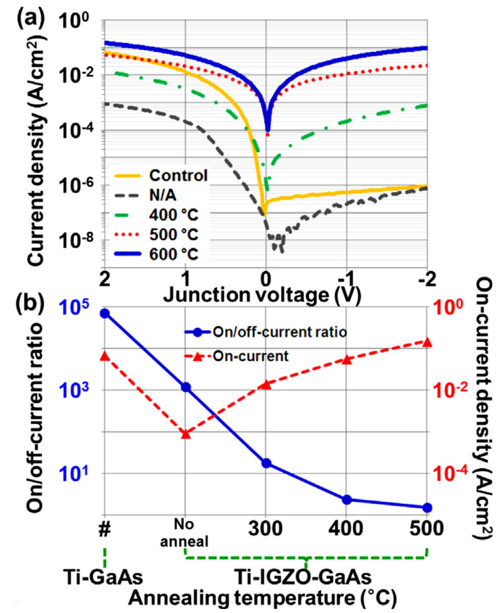

Fig. 5. (a) *J–V* characteristics of the Ti/n-GaAs (control) and Ti/IGZO/n-GaAs samples. (b) On/off-current ratio and on-current density of the Ti/n-GaAs (control) and Ti/IGZO/n-GaAs samples (extracted at $|V_A| = 2$ V).

4. Conclusion

In conclusion, we demonstrated a non-gold Ohmic contact on a low n-type GaAs substrate (~4×10^{16} cm^{-3}) by inserting thin IGZO layer. In order to precisely investigate the achieved Ohmic contact (Ti/IGZO on n-GaAs), TOF-SIMS, HSC chemistry, XPS, TEM, and *J–V* analyses were performed. After the annealing process above 400 °C, the diffused In reacted with As, forming InAs and InGaAs phases with lower energy bandgap than GaAs at the surface of GaAs substrate. As a result, it decreases the electron barrier height through the reduced energy bandgap, eventually increasing the reverse current. In addition, traps generated by the diffused O atoms also induced a trap-assisted tunneling phenomenon, increasing I_G and subsequently the reverse current. Therefore, an excellent Ohmic contact (0.15 A/cm^2 on-current density and 1.5 on/off-current ratio) was achieved on n-GaAs substrate by annealing at 600 °C and inserting IGZO layer.

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