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Research Article

Clean Interface Contact Using a ZnO Interlayer for Low-Contact-Resistance MoS_2 Transistors

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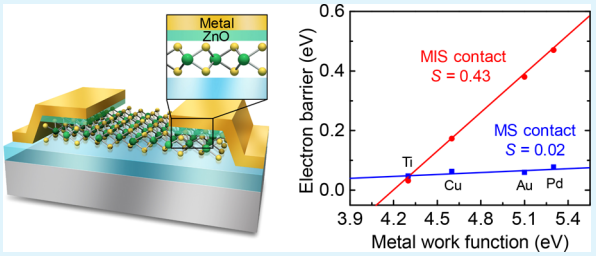
ABSTRACT: Two-dimensional transition metal dichalcogenides (TMDCs) have emerged as promising materials for next-generation electronics due to their excellent semiconducting properties. However, high contact resistance at the metal−TMDC interface plagues the realization of high-performance devices. Here, an effective metal−interlayer−semiconductor (MIS) contact is demonstrated, wherein an ultrathin ZnO interlayer is inserted between the metal electrode and MoS_2, providing damage-free and clean interfaces at electrical contacts. Using TEM imaging, we show that the contact interfaces were atomically clean without any apparent damages. Compared to conventional Ti/MoS_2 contacts, the MoS_2 devices with a Ti/ZnO/MoS_2 contact exhibit a very low contact resistance of 0.9 kΩ μm. These improvements are attributed to the following mechanisms: (a) Fermi-level depinning at the metal/MoS_2 interface by reducing interface disorder and (b) presence of interface dipole at the metal/ZnO interface, consequently reducing the Schottky barrier and contact resistance. Further, the contact resistivity of a Ti/ZnO/MoS_2 contact is insensitive to the variation of ZnO thickness, which facilitates large-scale production. Our work not only elucidates the underlying mechanisms for the operation of the MIS contact but also provides a simple and damage-free strategy for conventional aggressive metal deposition that is potentially useful for the realization of large-scale 2D electronics with low-resistance contacts.



KEYWORDS: *molybdenum disulfide, contact resistance, Schottky barrier height, zinc oxide, metal−interlayer−semiconductor structure*

INTRODUCTION

Over the past few decades, the success of semiconductor technology has been driven by continuous downscaling of Si transistors, and we are getting closer to their scaling limit. As it is becoming challenging to maintain a gate electrostatic control on the channel, the exploration of new materials suitable for further downscaling of transistors is essential to meet the demand of the semiconductor technology. Two-dimensional (2D) semiconductor materials such as transition metal dichalcogenides (TMDCs) are a promising alternative to Si due to their excellent gate modulation.[1,2] Among the various TMDCs, molybdenum disulfide (MoS_2) with a sizeable band gap, high mobility, and air stability allows for the realization of electronic and optoelectronic applications.[3]

Although MoS_2 field-effect transistors (FETs) exhibit excellent switching characteristics with a high on/off current ratio of 10^8 and subthreshold swing value (SS) of 65 mV dec^{-1},[4] the high resistance of the metal−MoS_2 interfacial contact remains a major challenge for the realization of a high-performance device.[5] This high contact resistance deteriorates the performance of the devices by introducing high operating voltages, low operating speed, and high power dissipation.[6] Various approaches have been proposed to improve the electrical contact on MoS_2,[7] such as phase engineering,[5] molecular/chemical doping,[8,9] and van der Waals contacts using mechanical transfer of metal thin-film electrodes.[10] The major issue in making low-resistance contacts on 2D MoS_2 is the presence of strong Fermi-level pinning at the metal−MoS_2 interface. This strong pinning is primarily due to the difficulty in fabricating an atomically clean metal−MoS_2 interface; typical processes for metal integration have been shown to cause severe damage to the 2D-layered MoS_2 and associated defect-induced gap states that pin the Fermi level at these energy levels.[10] Because of the Fermi-level pinning, Schottky barrier height (SBH) at the metal−MoS_2 junction tends to be constant, regardless of the work function of the metal. This incapability to modulate SBH has been a major hurdle for reduction of contact resistance.

A promising approach for modulating the SBH is the utilization of a metal−interlayer−semiconductor (MIS) contact structure, where an ultrathin interlayer is inserted between a metal and semiconductor. In this structure, the

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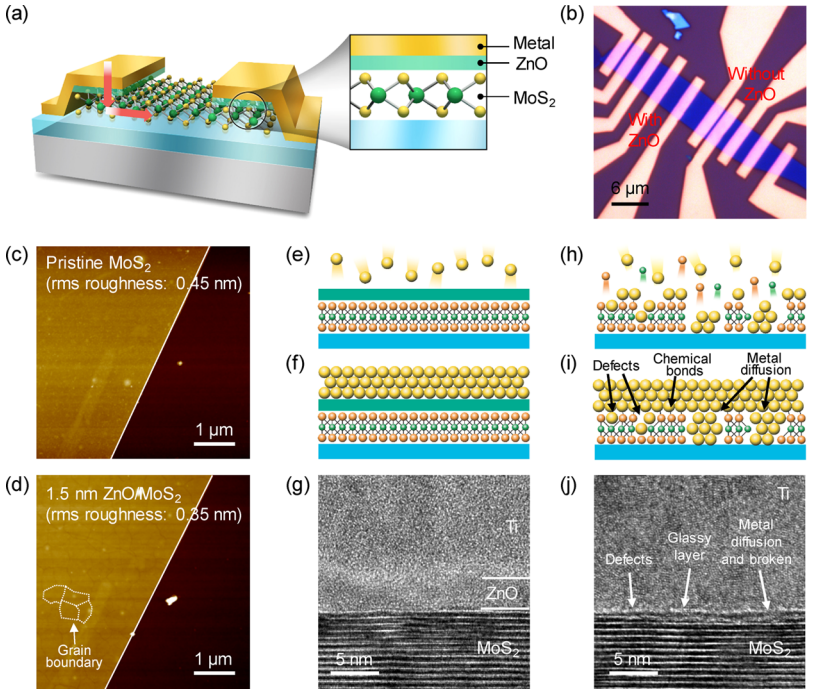

Figure 1. Schematic and structure characterization of MoS_2 transistors. (a) Schematic of the MoS_2 transistor with the ZnO interlayer. (b) Optical image of the MoS_2 device with and without the ZnO interlayer on the same flake. AFM images of the MoS_2 flake: (c) before and (d) after the atomic layer deposition (ALD) of 1.5-nm-thick ZnO. The solid line indicates the boundary between MoS_2 and SiO_2. The dashed line indicates the grain boundaries of ZnO. (e–g) Cross-sectional schematic and TEM image of the Ti/ZnO/MoS_2 contact, featuring clean metal–semiconductor interfaces. Here, the TEM image of a 3.5-nm-thick-ZnO-contacted device is shown for a better illustration because it is difficult to visualize a thinner ZnO due to electron beam damage during the TEM imaging. (h–j) Cross-sectional schematic and TEM image of the conventional Ti/MoS_2 contact, where the few topmost MoS_2 layers can be damaged by evaporated metals, resulting in considerable interface disorder.

interlayer serves as a protective buffer layer, providing a clean interface and preventing the Fermi-level pinning;[11,12] thus, a low-resistance contact can be obtained by lowering the Schottky barrier between the low-work-function metal and MoS_2. Previous studies have shown that creation of MIS contacts using a Ta_2O_5,[13] TiO_2,[14,15] MgO,[16] and hexagonal boron nitride (h-BN)[17] interlayer can improve the contact properties on MoS_2. However, most studies have focused on the improvement induced by the reduction of SBH at contacts; the underlying mechanism is not clearly understood, which has hindered further developments. Furthermore, the incorporation of interlayers, including Ta_2O_5 and h-BN,[13,17] causes the contact resistance to be strongly dependent on interlayer thickness due to an unavoidable tunneling resistance, which is unfavorable in terms of a process window and variation standpoint for large-scale production.

Here, we demonstrate the fabrication of metal–interlayer–semiconductor contacts, where an ultrathin ZnO layer is inserted to serve as the physical buffer layer, providing an interface free of the interface disorder and Fermi-level pinning. We use transmission electron microscopy (TEM) to show that the contact interfaces were atomically clean without any apparent defects. With the optimized Ti/ZnO/MoS_2 contact, we achieved a low contact resistance of 0.9 kΩ μm at 300 K for a carrier density (n) of 3.0×10^{12} cm^{-2}. This contact resistance value is comparable to and even lower than previously reported MoS_2 contact strategies (Table S1, Supporting Information). We have validated that the low contact resistance is attributed to the synergistic effects of Fermi-level depinning and interface dipole at the interfaces. In addition to the observed contact improvement, the contact resistivity of the Ti/ZnO/MoS_2 contact is insensitive to the thickness of the ZnO interlayer, permitting an excellent process window (~4 nm) for the realization of large-scale and complementary metal–oxide–semiconductor (CMOS)-compatible manufacturing.

RESULTS AND DISCUSSION

The fabrication procedure for the MoS_2 FETs with a ZnO interlayer is schematically shown in Figure S1 (Supporting Information), and the experimental conditions are described in detail in the Methods section. Briefly, multilayered MoS_2 flakes (6–13 nm) were prepared by mechanical exfoliation onto a 285-nm-thick SiO_2/Si substrate. Next, source/drain contact regions were patterned by e-beam lithography and development, leaving the exposed contact regions for subsequent deposition of the ZnO interlayer. The ZnO layer was uniformly deposited at a low temperature of ~90 °C using the plasma-enhanced atomic layer deposition (PEALD). The final device was obtained by depositing the contact metal using an e-beam evaporator, resulting in the formation of the MIS contacts. Figure 1a presents a schematic of the fabricated MIS contact consisted of a metal/ZnO/MoS_2 heterostructure. Figure 1b shows an optical image of the fabricated device. In this structure, the underlying MoS_2 is in contact with the bottom part of the ZnO layer, while the top part of the ZnO layer is in contact with the metal electrodes. The path for electron transports is denoted by arrows, indicating electron tunneling (vertical direction) from the source to MoS_2 through the ZnO interlayer and then drift diffusion (lateral direction) through the MoS_2 layer. The electrons can effectively tunnel through a few nm-thick ZnO interlayer and thus contribute to the total current.

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Table 1. Material Properties of Various Interlayers[a] and Calculated Conduction Band Offsets[b]

interlayer	band gap (eV)	dielectric constant	electron affinity (eV)	conduction band offset (eV)
Al_2O_3	6.1	9	1.0	3.28
Ta_2O_5	4.5	25	3.7	0.58
TiO_2	3.2	80	4.2	0.08
ZnO	3.4	10	4.3	−0.02

[a]The material parameters were obtained from those previously reported in the literature.[13,21] [b]The calculated conduction band offsets are extracted by subtracting the electron affinity of multilayered MoS_2 from the electron affinity of the interlayer.

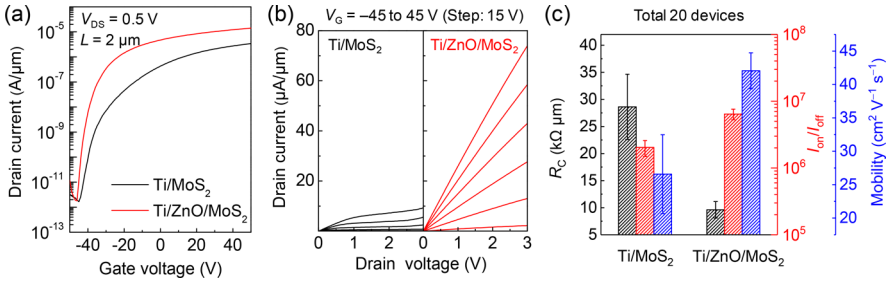

Figure 2. Electrical properties of MoS_2 transistors. (a) Transfer and (b) output characteristics of MoS_2 FETs with Ti/MoS_2 and Ti/ZnO/MoS_2 contacts. (c) Contact resistance, on/off current ratio, and two-terminal field-effect mobility of MoS_2 FETs with Ti/MoS_2 and Ti/ZnO/MoS_2 contacts, obtained from twenty different devices.

This ZnO interlayer at MIS contacts offers several advantages over conventional metal−semiconductor (MS) contacts and other interlayer materials. First, the insertion of the ZnO interlayer at contacts provides a gentle metal integration without damaging the MoS_2 layer; the thin ZnO interlayer acts as the physical buffer layer protecting the underlying MoS_2 from high-energy metal deposition, thereby reducing the interface disorder and the Fermi-level pinning. Second, the low conduction band offset (CBO) between the ZnO and MoS_2 offers a favorable electrical band alignment between them to minimize the tunneling resistance. In general, the insulating interlayer may cause an additional tunneling resistance because electron tunneling is strongly dependent on the barrier height and width of the interlayer.[18] Therefore, it is essential to obtain a thin interlayer with appropriate energy levels sandwiched between the contact metal and MoS_2. Theoretical studies have suggested the use of interlayer materials with low CBO to MoS_2, such as TiO_2 and ZnO, to achieve a low-resistance MIS contact without introducing significant tunneling resistance.[19−21] Inspired by this, we have considered ZnO as an ideal candidate over the other widely used interlayer materials because the CBO between ZnO and multilayered MoS_2 is very low to be zero (−0.02 eV; Table 1; Figure S12, Supporting Information). This enables the creation of a remarkably small tunneling barrier with a large conduction band overlap at the metal−MoS_2 junction, which can permit a highly efficient tunneling of the electrons through the ZnO interlayer. Third, physical separation between the metal and MoS_2 without any direct chemical bonding can also suppress the metal-induced gap states and pinning effect.[10]

Before device fabrication, the ZnO/MoS_2 interface was extensively characterized to assure the exact MIS contact structure as designed. This is essential for ensuring the high-quality MIS contact, as the performance of the contact is limited by the incomplete surface coverage of the interlayer.[22] In the case of incomplete surface coverage, the deposition of high-energy metals can lead to substantial damage to the underlying MoS_2 and cause the interface disorder, creating the defect-induced gap states that results in Fermi-level pinning, and, consequently, the device performance is degraded. The atomic force microscopy (AFM) scan shows that the 1.5-nm-thick ZnO film has a uniform and complete coverage on MoS_2 (Figure 1c, d; Figure S2 for 3.5-nm-thick ZnO, Supporting Information). The ultrathin ZnO layer entirely covered the MoS_2 surface, in which emerging grains show a well-connected morphology with clearly defined grain boundaries. The root-mean-square (rms) roughness of the 1.5-nm-thick ZnO/MoS_2 (0.35 nm) is also comparable to that of the pristine MoS_2 (0.45 nm). Cross-sectional TEM images further verified that the ZnO layer was uniformly deposited and formed an intimate contact with the MoS_2 layer (Figure 1g; Figure S3 for lower magnification image; Figure 1j for clear comparison). It is important to note that the use of the PEALD technique is critical for obtaining an ultrathin and continuous ZnO layer without significant lattice damage or surface oxidation of MoS_2, as confirmed by Raman spectroscopy (Figure S4, Supporting Information). Therefore, this ZnO/MoS_2 heterostructure can provide the basis for the successful operation of the MIS contact described in the following sections.

After device fabrication, we investigated the effect of the ZnO interlayer on contact quality with electrical transport measurements (Figure 2). The Ti/MoS_2 and Ti/ZnO (2 nm)/MoS_2 contacts were fabricated on the same MoS_2 flake to compare the two contact structures under the same condition, as shown in Figure 1b. We used Ti as the contact metal, which has a low work function (4.3 eV), to align the Fermi level with the conduction band edge of MoS_2 for electron injection. First, the transfer characteristics were evaluated by modulating the silicon back-gate bias (Figure 2a). Here, the two-terminal field-effect mobility (including the contact resistance) was extracted at V_{DS} = 0.5 V from the linear region of the transfer curve using the equation $\mu_{FE} = L/(WC_{OX}V_{DS}) \times (\partial I_{DS}/\partial V_{GS})$, where L, W, V_{DS}, and V_{GS} are the channel length, channel width, drain voltage, and back-gate voltage, respectively, and the capacitance per unit area (C_{OX}) is $\varepsilon_{OX} \times \varepsilon_0/t_{OX}$, with a relative permittivity (ε_{OX}) of 3.9 for SiO_2. For the conventional Ti/MoS_2 contact, the device exhibited a typical n-type behavior with an on/off current ratio of 1.8×10^6 and field-effect

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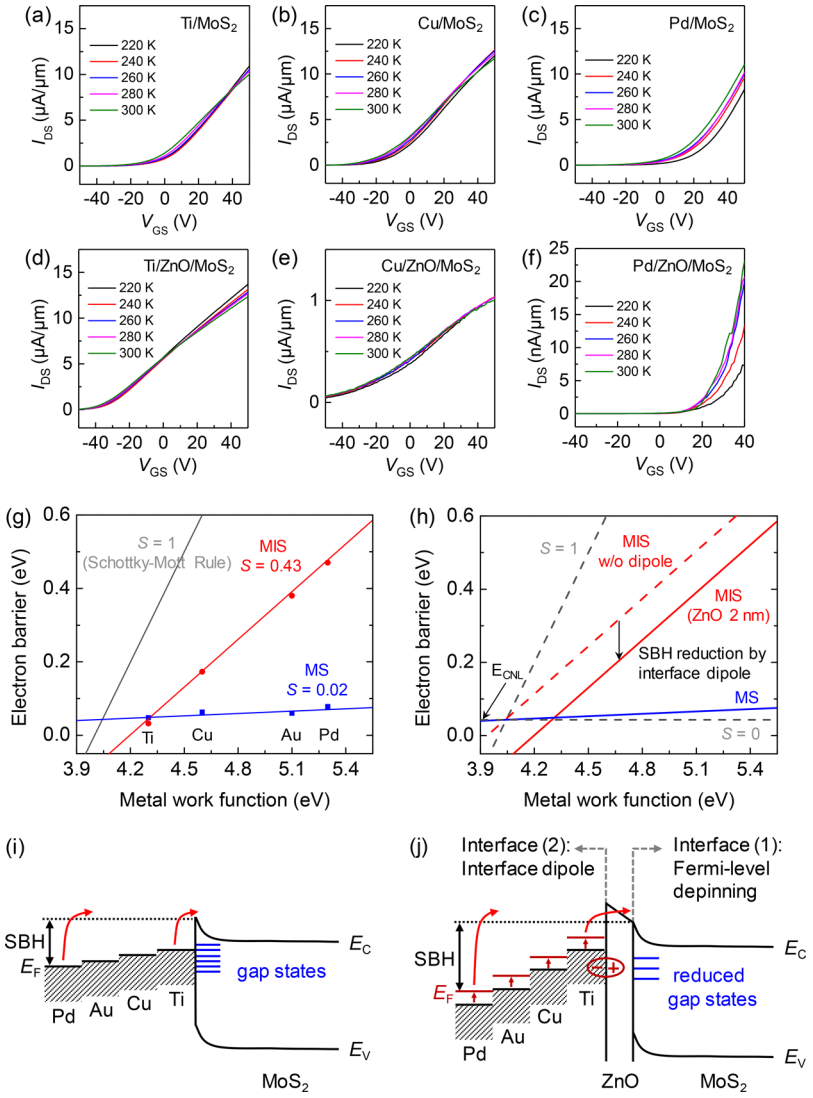

Figure 3. Temperature dependence of electrical property and SBH. I_{DS}–V_{GS} transfer curves of MoS_2 transistors with conventional (a) Ti, (b) Cu, and (c) Pd electrodes. I_{DS}–V_{GS} transfer curves of MoS_2 transistors with ZnO-contacted (d) Ti, (e) Cu, and (f) Pd electrodes. (g) SBH and (h) fitted lines for MS and MIS contacts versus work function of the contact metal, obtained from Figure S10 in the Supporting Information. Schematic energy band diagrams of multilayered MoS_2 for the (i) MS and (j) MIS contact with different metal contacts. All electrical measurements were performed for long-channel transistors ($L \approx 2$ μm) at a low drain bias (V_{DS} = 0.5 V)

mobility of 22.7 cm^2 V^{-1} s^{-1}, similar to the previously reported values for MoS_2 devices with Ti/Au.[23] After the ZnO interlayer is inserted at the source/drain contact, the device exhibited an improved on/off current ratio of 7.3 × 10^6 and field-effect mobility of 66.2 cm^2 V^{-1} s^{-1}. Furthermore, the maximum on-current density was increased by a factor of ~7 (from 9 to 70 μA μm^{-1} at V_{DS} = 3 V) due to the insertion of the ZnO interlayer (Figure 2b). For a clear estimation of the device improvement, we performed a statistical analysis by fabricating twenty different devices (Figure 2c). Specifically, the Ti/ZnO/MoS_2-contacted transistor shows the on/off current ratio of 6.42 × 10^6 ± 0.5 × 10^6 and the mobility of 42.05 ± 2.7 cm^2 V^{-1} s^{-1}, whereas the Ti/MoS_2-contacted transistor shows the on/off current ratio of 2.03 × 10^6 ± 1.15 × 10^6 and the mobility of 26.57 ± 5.9 cm^2 V^{-1} s^{-1}. The statistical results strongly suggest that a reproducible and consistent performance enhancement can be achieved by the proposed method. Besides the observed device improvement, it is particularly important to note that the use of the ZnO interlayer enhances the on/off current ratio while retaining a low off-state current. This is in striking contrast to the molecular/chemical doping of MoS_2, where the fabricated transistors are not completely turned off due to degenerate-like doping, leading to a low on/off current ratio.[8,9] With our approach of inserting the ZnO interlayer, a high on-current density and a high on/off current ratio are simultaneously achieved, which is essential for the realization of high-performance logic circuits.

We note that these improvements are generally accompanied by a lower threshold voltage (V_{TH}) in the Ti/ZnO/MoS_2 contact compared to that in the Ti/MoS_2 contact. As shown in Figure 2a, the insertion of the ZnO interlayer causes a manageable V_{TH} shift of ~23 V, estimated by linear extrapolation from each transfer curve (Figure S6, Supporting Information), as reported previously.[13,17] The rather low V_{TH} may be attributed to the reduction of contact resistance due to the use of the conventional SiO_2/Si back-gate structure, which led to an increase in the effective gate bias ($V_{GS,eff} = V_{GS} - R_C I_{DS}$).[24,25] We performed the transfer length measurements

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(TLM) to quantitatively investigate the contact resistance (details in Supporting Information, section 4). The Ti/ZnO/MoS_2 contact exhibits lower contact resistance (6.6 ± 0.2 kΩ μm at a carrier density $n = 4.0 \times 10^{12}$ cm^{-2}) compared with that of a typical Ti/MoS_2 contact (25.65 ± 2.8 kΩ μm). Similar improvements were also observed in other Ti/ZnO/MoS_2 contact samples, with contact resistances near 10 kΩ μm at high carrier density (Figure 2c). Furthermore, we achieved the lowest contact resistance of 0.9 kΩ μm at $n = 3.0 \times 10^{12}$ cm^{-2} for our best sample (Figure S9, Supporting Information); this contact resistance value is lower than the values obtained using an h-BN[17] and TiO_2 interlayer[14] but slightly larger than the values achieved by MoS_2 phase engineering[5] and the Ni/graphene contact[26] as summarized in Table S1 in the Supporting Information. Taken together, these results clearly demonstrate that the insertion of the ZnO interlayer at the contact can effectively reduce the contact resistance, which consequently improves the device on/off current ratio and carrier mobility.

To understand the role of the ZnO interlayer at the metal/MoS_2 interface in reducing the contact resistance, we conducted a systematic analysis of the primary factors affecting the contact resistance, that is, (i) the doping effect and (ii) the effect of SBH modulation. (i) Considering the fact that thinning the Schottky barrier by increasing the doping density at or near the contact is a common practice in conventional FETs,[27] the ZnO layer may induce n-doping of the underlying MoS_2 layer via surface charge transfer.[14,15] As we did not observe any signature of n-doping in MoS_2 during the ZnO deposition process from both Raman and photoluminescence analyses (Figures S4 and S5, Supporting Information), we can rule out ZnO-induced doping as a primary mechanism. (ii) Because the contact resistance is exponentially proportional to the SBH, the reduction of contact resistance can be attributed to lowered SBH across the metal−MoS_2 junction.[28] Indeed, such modulation of SBH has been experimentally reported in MoS_2 devices using various interlayers.[13−17] However, most of the earlier studies have been limited to specific phenomena, such as the reduction of SBH; little attention has been paid to understand the mechanism through which the Fermi-level depinning affects the SBH modulation.

To this end, we carried out temperature-dependent studies by employing several contact metals with different work functions (W_M): Ti ($W_{Ti} \approx 4.3$ eV), Cu ($W_{Cu} \approx 4.6$ eV), Au ($W_{Au} \approx 5.1$ eV), and Pd ($W_{Pd} \approx 5.3$ eV). Figure 3a−f presents the $I_{DS} - V_{GS}$ transfer curves of MoS_2 devices using a series of MS structures with different work functions, along with a comparison of results for the MIS contacts. As shown in Figure 3a−c, the MoS_2 devices contacted by typical metals exhibit similar transfer characteristics as well as high on-state current levels, independent of the work function of the metal. This indicates that the Fermi level is strongly pinned near the conduction band edge and can be barely modulated by the metal work function. By contrast, MIS-contacted MoS_2 devices exhibit tunable electrical properties that are governed by the work function of the metal (Figure 3d−f). For instance, well-behaved n-type transport can be achieved for Ti (Figure 3d), which has a low work function, with a clear metal−insulator transition behavior[17] and high on-state current, indicating a low contact barrier. With increasing the work function by employing Pd, the device exhibits a poor n-type characteristic with a low on-state current level (a few tens of nanoamperes) (Figure 3f); I_{DS} is three orders of magnitude smaller than that of a conventional Pd-contacted device. I_{DS} also exhibits a relatively large temperature dependence, suggesting that the high contact barrier dominates the overall carrier transport.

The transport measurements with variable temperature further allowed us to estimate the SBH across the metal−MoS_2 junction, which is explained in more detail in Figure S10 (Supporting Information). Figure 3g summarizes the measured SBH for various contact metals as a function of their work functions. Here, the degree of Fermi-level pinning was characterized by the pinning factor S ($S = |d\Phi_{SB}/dW_M|$), which is indicated by the solid lines. In general, S varies from 1 for unpinned interfaces (Schottky−Mott rule) to 0 for completely pinned states.[29] For the MoS_2 devices with the MS contact, the extracted value of S is 0.02 with nearly constant SBH, indicating strong Fermi-level pinning.[10] In contrast, for the MoS_2 devices with the MIS contact, the value of SBH largely depends on the work function; SBH increases with the increase in the work function of the metal. The fitted S value for MIS contact is 0.43, which is much larger than that for MS contact, indicating that significant Fermi-level depinning is induced by the ZnO interlayer. The S factor does not reach 1, indicating that the Fermi level pinning is not perfectly alleviated. The reasons for this are thought to be as follows: (i) remaining gap states due to oxidation of the MoS_2 surface. The oxidation should proceed via a chemical reaction between the MoS_2 and adsorbed water molecules during the device fabrication, which was conducted in ambient air. (ii) Insufficient ZnO thickness to fully prevent the metal penetration.

This large discrepancy in the value of S between the MS and MIS contacts arises from the interface disorder, largely due to the aggressive fabrication process and the fact that the low-resistance contact in the MoS_2 device can only be obtained after achieving clean and intact metal−MoS_2 interfaces;[10,11,30] in other words, the value of S and thus the pinning effect is strongly dependent on the metal−MoS_2 interface cleanliness. To confirm the effect of the interface state on pinning, we used cross-sectional TEM to analyze the interface. Figure 1g clearly shows that the ZnO/MoS_2 interface becomes practically clean without any apparent defects on MoS_2, whereas the metal/MoS_2 interface (Figure 1j; Figure S3 for lower magnification image, Supporting Information) shows considerable disorder such as atomic displacement, broken layer, metal diffusion, and chemical intermixing (between the few topmost MoS_2 layers and contact metal). These observations suggest that the complete passivation of MoS_2 by the ZnO interlayer can provide sufficient protection, which significantly reduces the number of defects at the interface. Consequently, the defect-induced gap states and thus the pinning effect is reduced.[10] The clean interface is further supported by the enhancement of the SS value, which is strongly related to the interface trap densities at or near the contact in TMDC-based transistors (Figure 2a; Figure S8, Supporting Information).[31,32] Therefore, the ability to create atomically clean contact interfaces and to modulate the SBH opens a way to alleviate the pinning effect and to improve contact properties.

In addition to the Fermi-level depinning, the presence of interface dipole at the metal/ZnO interface can also induce shifts in the Fermi level of the contact metal, thereby leading to additional modulation of SBH. As shown in Figure 3h, we separated the effects of Fermi-level depinning and interface dipole. The intersection point between the MS contact line with $S = 0.02$ and the ideal contact line with $S = 1$ yields the

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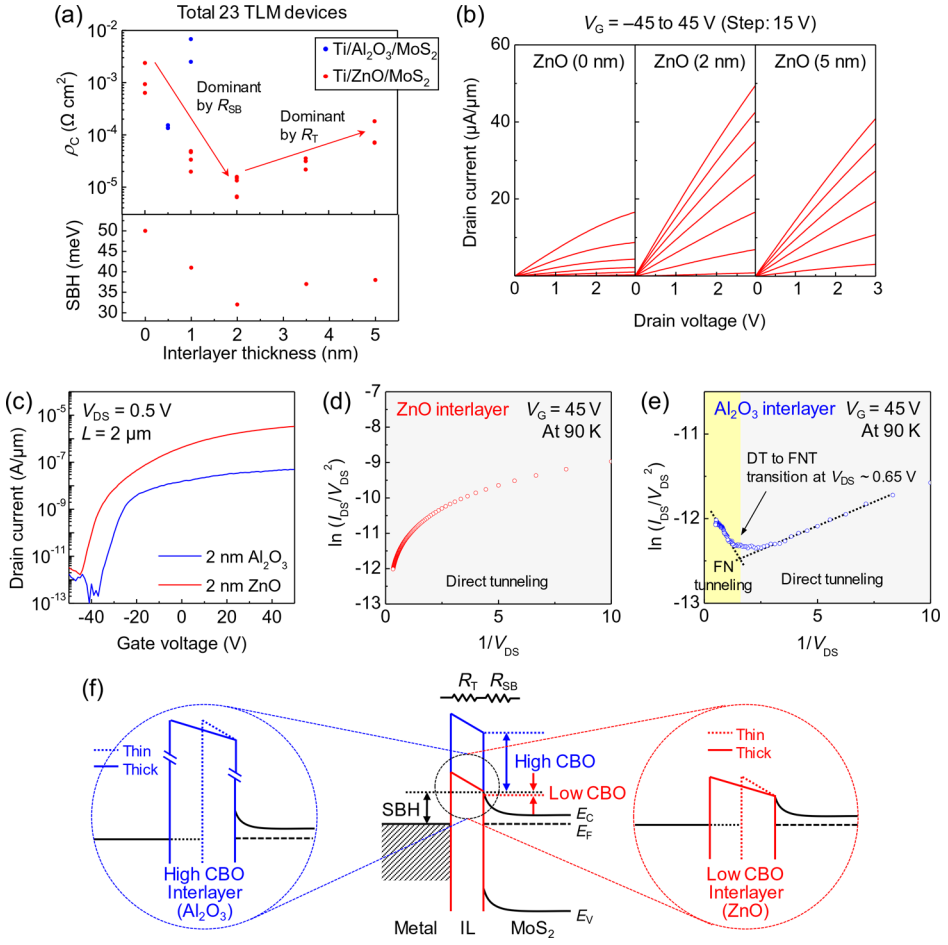

Figure 4. Dependence of interlayer thickness and CBO on the MIS contact. (a) Specific contact resistivity and SBH as a function of interlayer thickness, obtained from at least three different TLM devices for each condition. (b) Linear output characteristics of MoS_2 FETs for varying ZnO thickness. The channel length of the measured devices is 2 μm. (c) Transfer characteristic of MoS_2 FETs with the ZnO interlayer and that with the Al_2O_3 interlayer for comparison. (d, e) ln (I/V^2) versus $1/V$ curves for ZnO and Al_2O_3 interlayer, respectively. (f) Schematic band diagram of the MIS contact structure depicting the cases of high and low CBO.

branch point and the experimental value of charge neutrality level (E_{CNL}), which is 40 meV below the conduction band edge.[33] Meanwhile, the MIS contact line must cross the branch point, but it generally does not. This deviation arises from another factor that is hard to avoid interactions at the interface between two dissimilar materials, and the factor is the presence of interface dipole at the metal/ZnO interface.[22] Such interface dipole induces a parallel up-shift in the Fermi level of the metals, lowering the SBH of the metal–MoS_2 contact, which is in agreement with an earlier study.[33] The energy band diagrams of the MS and MIS contact structures are illustrated in Figure 3i,j. To summarize the above discussion, we concluded that the mechanism for the role of the ZnO interlayer follows the combined effects of the Fermi-level depinning and the interface dipole, which have been applied here to explain the device improvement in the Ti/ZnO/MoS_2 contact system; the ZnO interlayer lowers the SBH of the Ti–MoS_2 contact, which in turn reduces the contact resistance. We believe that a further reduction of SBH in the ZnO-contacted device can be attained by employing contact metals with low work function, such as Sc[3], In,[30] and Al.[34]

The ability to modulate the contact resistance through control of the ZnO thickness provides a path toward the rational design and large-area electronics based on MIS contacts. Figure 4a shows the specific contact resistivity (ρ_C) for the Ti/ZnO/MoS_2 contact as a function of ZnO thickness. To obtain good statistical results, at least three different TLM devices were analyzed for each thickness. ρ_C exhibited a significant decrease as the ZnO thickness increased from 0 to 2 nm. However, after reaching the lowest ρ_C of 6×10^{-6} Ω cm^2 at a thickness of 2 nm, ρ_C exhibited a slight increase. Similar interlayer thickness dependence of ρ_C has been reported for other 2D semiconductor FETs with a Ta_2O_5 or Al_2O_3 interlayer, where models considering the additional tunneling resistance were invoked to account for the observed valley-curve trend.[13,35] Simply speaking, the contact resistance (R_C) of the MIS contact can be described by two resistances in series: (i) the Schottky barrier resistance (R_{SB}), which depends on the SBH of the metal–MoS_2 junction as well as the depletion width of MoS_2 and (ii) the tunneling resistance (R_T), which depends on the tunneling barrier formed by the interlayer. Because of the competition between the decrease in R_{SB} (via Fermi-level depinning and interface dipole as discussed above) and the increase in R_T with increasing ZnO thickness, the optimal thickness is determined by a trade-off between these factors, as represented by the arrows in Figure 4a. Without the ZnO interlayer, the highly pinned and large SBH (~50 meV) causes R_{SB} to dominate the overall contact resistivity in the range of $10^{-3} - 10^{-4}$ Ω cm^2. With a thin ZnO interlayer present, the Fermi-level depinning along with

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interface dipole effect greatly reduces the SBH across the metal−MoS_2 junction and the depletion width, which allows the electrons to easily overcome the contact barrier through thermionic emission and thermionic field emission.[6,36] This results in a large reduction of R_{SB}, such that the overall contact resistivity is decreased dramatically. However, once the thickness of ZnO interlayer is increased beyond an optimal value (2 nm), R_T starts to dominate the carrier transport, and the current becomes tunneling-limited, leading to the increased contact resistivity despite the low SBH. We further tested the device using the ZnO layer with a larger thickness of 7 nm (Figure S11, Supporting Information). The thick depletion width of ZnO significantly limits the current flow, which results in an on-current density that is approximately 2 orders of magnitude smaller than that in an optimized device.

Despite this, our ZnO interlayer has a distinct advantage over the previously reported interlayer materials: its insensitivity of contact resistivity to the interlayer thickness that could enable large-area fabrication. When fabricating a large batch of MoS_2 devices on a substrate, it is crucial to achieve a good device-to-device uniformity across the wafer. Strong thickness sensitivity leads to a corresponding variation in the contact property of MoS_2 transistors, causing a large variation in the device performance. Recently, a Ta_2O_5-contacted device was investigated, but the strong thickness sensitivity resulted in a narrow process window of ∼1 nm (1.5 to 2.5 nm); the contact resistivity sharply increased by two orders of magnitude when the thickness was increased from 1.5 to 5 nm.[13] On the contrary, our ZnO-contacted device offers a reasonably wide process window of ∼4 nm (1 to 5 nm, Figure 4a); the contact resistivity is maintained within one order of magnitude in the thickness from 1 to 5 nm, suggesting a sufficient margin for CMOS-compatible manufacturing. As shown in Figure 4b, high on-current density is also maintained even in a rather thick interlayer (5 nm).

This large difference can be attributed to different CBO between the interlayers and MoS_2.[37] To further confirm the effect of CBO on the contact properties, we also studied MoS_2 devices with MIS contacts containing an Al_2O_3 interlayer for comparison. The CBO of ZnO and the Al_2O_3 interlayer are −0.02 and + 3.28 eV, respectively (Table 1; Figure S12, Supporting Information). Figure 4a shows the contact resistivity measured in an Al_2O_3-contacted device as a function of thickness, which clearly exhibits a sharp dip around the thickness of 0.5 nm and a relatively narrow process window (<1 nm). In addition, the charge injection through an even 2-nm-thick Al_2O_3 interlayer severely limits the on-current density, indicating high contact resistance (Figure 4c). We used the approach of direct tunneling (DT) and Fowler−Nordheim tunneling (FNT) models in order to estimate the tunneling barrier height.[38] At low temperature, the $\ln(I/V^2)$ versus $1/V$ plot will exhibit logarithmic dependence in the DT (at low bias) regime and linear dependence with a negative slope in the FNT (at high bias) regime. Figure 4d,e shows the plots corresponding to $\ln(I/V^2)$ versus $1/V$ with a gate bias of 45 V (device on state) and a low temperature of 90 K. Only the DT regime was observed for the 2-nm-thick ZnO interlayer (Figure 4d), whereas both DT and FNT regimes were observed for the 2-nm-thick Al_2O_3 interlayer (Figure 4e) with a clear transition between them at $V_{DS} \approx 0.65$ V. Such a transition from the DT to FNT regime in the Al_2O_3-contacted device is a signature of high tunneling barrier at the metal−MoS_2 junction. We also discuss the dependence of ZnO thickness on the carrier injection mechanism in more detail in Figure S13 (Supporting Information).

Finally, based on the above analyses, we can approximately draw the energy band diagrams in Figure 4f, depicting the cases of high-CBO (Al_2O_3) and low-CBO (ZnO) interlayers. Before applying the bias, the initial tunneling barrier is determined by the CBO between the interlayer and MoS_2. For the high-CBO interlayer, small potential drop at the interlayer/MoS_2 interface forms a trapezoidal energy barrier. In this case, the effective barrier width is increased with the increase in the interlayer thickness, resulting in a large increase in the tunneling resistance and thus the contact resistivity. By contrast, for the low-CBO interlayer, large drop in the electrical potential creates a triangular barrier in which the effective barrier width is small. Thus, the increase in the interlayer thickness does not cause a significant increase in the effective barrier width and tunneling resistance, and, hence, the contact resistivity is less sensitive to the interlayer thickness. This ability to pose the wide process windows is an important advantage of our ZnO approach, which is potentially useful for the large-area fabrication of MoS_2 transistors on a single chip.

CONCLUSIONS

In this paper, we demonstrated a clean interface contact by inserting the ZnO interlayer between MoS_2 and metal electrodes in MoS_2-based FETs for the first time. Using TEM imaging, we showed that the contact interfaces were atomically clean without any apparent damages, suggesting defect-free interfaces at the contacts. With the optimized Ti/ZnO/MoS_2 contact, the MoS_2 devices exhibited an excellent performance including a contact resistance of 0.9 kΩ μm (at $n = 3.0 \times 10^{12}$ cm^{-2}) and a wide ALD process window of ∼4 nm, which is a critical advancement over the previously reported devices with other interlayer materials. These improvements are attributed to the Fermi-level depinning at the interfaces as well as the low CBO between ZnO and MoS_2, which lowers the contact barrier across the Ti−MoS_2 junctions. Our work provides a simple strategy for fabricating clean interface contacts to realize high-performance 2D electronics and optoelectronic devices.

METHODS

Fabrication of MoS_2 FETs with a ZnO Interlayer. Multilayered MoS_2 flakes (6−13 nm) were obtained via the scotch tape method, which were subsequently transferred onto a highly doped silicon substrate with a 285-nm-thick SiO_2 layer that served as the bottom gate and gate dielectric, respectively. The contact regions were patterned by the standard electron-beam lithography technique (ELPHY Plus and Quantum, Raith) using a polymethyl methacrylate (PMMA) resist (A6 950k, Microchem). We used plasma-enhanced atomic layer deposition (PEALD; ISAC Research Inc.) for depositing the ZnO interlayer. Finally, various metal electrodes (15 nm Ti, Cu, Au, and Pd) capped with 30 nm Au were deposited by e-beam evaporation (KVE-E2000, Korea Vac) for electrical measurements. For comparison, control devices without the ZnO interlayer were fabricated using the same procedure. Unless otherwise specified, the channel length of two-terminal MoS_2 FETs was 2 μm.

Characterization. Atomic force microscopy (AFM; XE-100, Park Systems) and Raman spectroscopy (LabRAM HR Evolution, Horiba Jovin-Yvon) with a laser wavelength of 514 nm were used to characterize the surface properties of MoS_2 flakes. Photoluminescence (alpha300 M+, WITec) and Raman spectroscopy were carried out to investigate the interaction between the ZnO and MoS_2 layer. High-resolution TEM images of the cross sections of MoS_2 flakes were obtained using an image aberration-corrected TEM (HF-3300,

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Hitachi). All the electrical measurements of the devices were conducted using a semiconductor parameter analyzer (4155C, Agilent Technologies) in vacuum (~10^{-2} torr) at 80−373 K.

■ ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acsami.9b18591.

Fabrication of MoS_2 FETs with the ZnO interlayer, characterization techniques, contact characterization, estimation of Schottky barrier height, Figures S1−S13, Table S1, and references (PDF)

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Notes

The authors declare no competing financial interest.

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